What is claimed is:

1. A scan test system for a semiconductor device, comprising:

a first semiconductor device including a first analog input/output pin existing on the analog input side thereof, a first internal circuit, and a scan register connected between said first input/output pin and said first internal circuit;

a second semiconductor device including a second analog input/output pin on the analog input side thereof, a second internal circuit, and a scan register connected between said second input/output pin and said second internal circuit; and

an analog wiring connecting said first analog input/output pin and said second analog input/output pin.

2. The scan test system for a semiconductor device according to Claim 1, wherein at least one of the first and second semiconductor devices constitutes a register chain that serially connects a plurality of the scan registers within the device.

3. The scan test system for a semiconductor device according to Claim 2, wherein the scan register constituting the register chain complies with the JTAG specification, and constitutes a JTAG scan register, and the test system comprises control means for controlling this JTAG scan register.

4. A scan test system for a semiconductor device, comprising:

said semiconductor device including:

a first scan register connected between a digital/analog double function pin on the input side and an internal circuit;

a second scan register connected between a digital input/output pin and said internal circuit;

a first register chain serially connecting a plurality of said first scan registers, each fetching the data input and outputting the result to the output side;

a second register being connected to said first register chain and simultaneously serially connecting a plurality of said second scan registers, each fetching the data input and outputting the result to the output side; and

switching means bypassing at least one of said first and the second register chains and thereby connecting the data input to the output side.

5. A scan test system for a semiconductor device according to Claim 4, wherein the scan register constituting the first and the second register chains complies with the JTAG specification, and constitutes a JTAG scan register, and the test system comprises control means for controlling this JTAG scan register.

6. A scan test system for a semiconductor device according to Claim 4, wherein the switching means comprises: a first switch, a first bypass line that bypasses the first register chain, a second switch and a second bypass line that bypasses the second register chain, the first switch switches between the first register chain and the first bypass line, and the second switch switches between the second register chain and the second bypass line.